***** WARNING *** HIGH VOLTAGE POTENTIAL *** WARNING *****

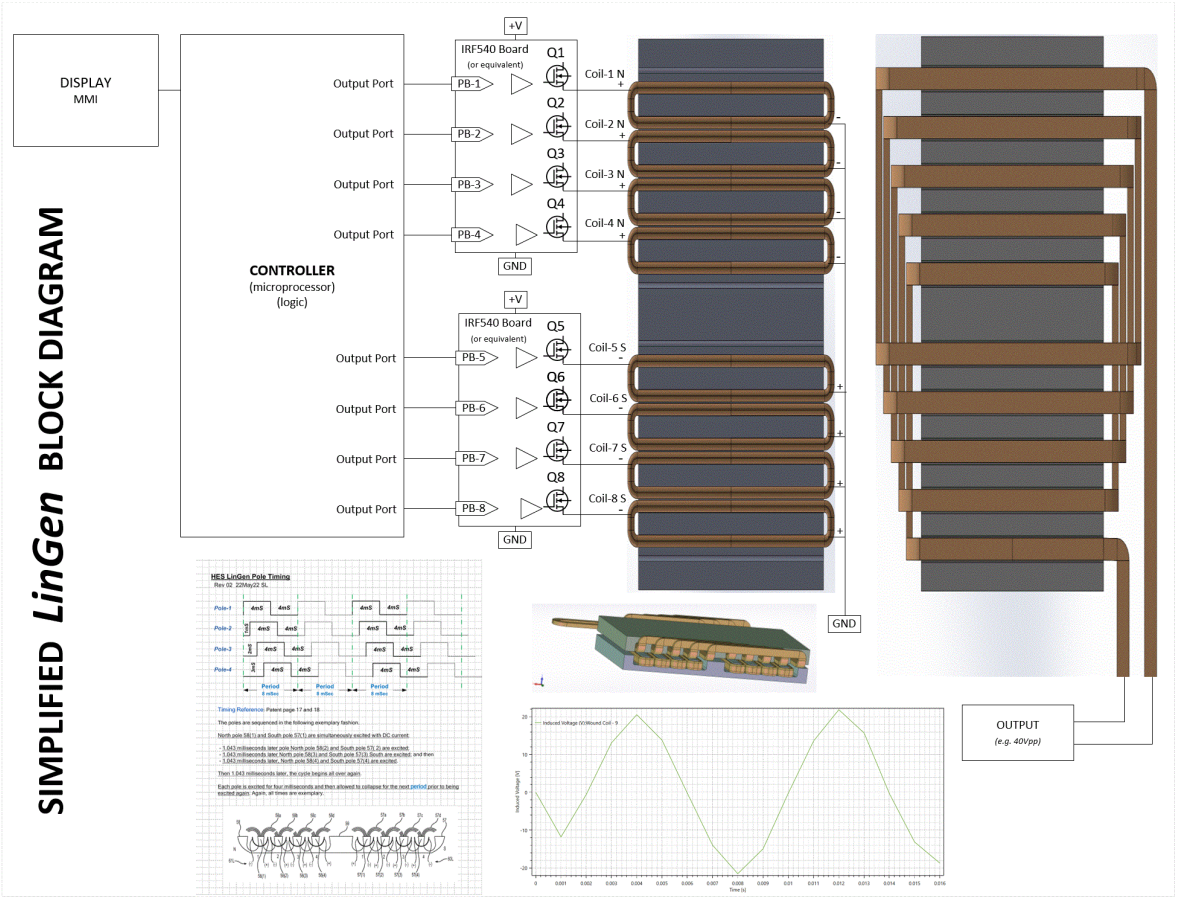
LINGEN SIMULATION (based on the original design investigation/analysis from Patent)

A "bench test" anomaly that appeared to be an excessive high voltage at the output was observed when testing a partial diode-capacitor kludge (see schematic). This kludge was added in the simulation for further (safe) study and analysis. The results are shown below in "CAP Voltage Plot 3."

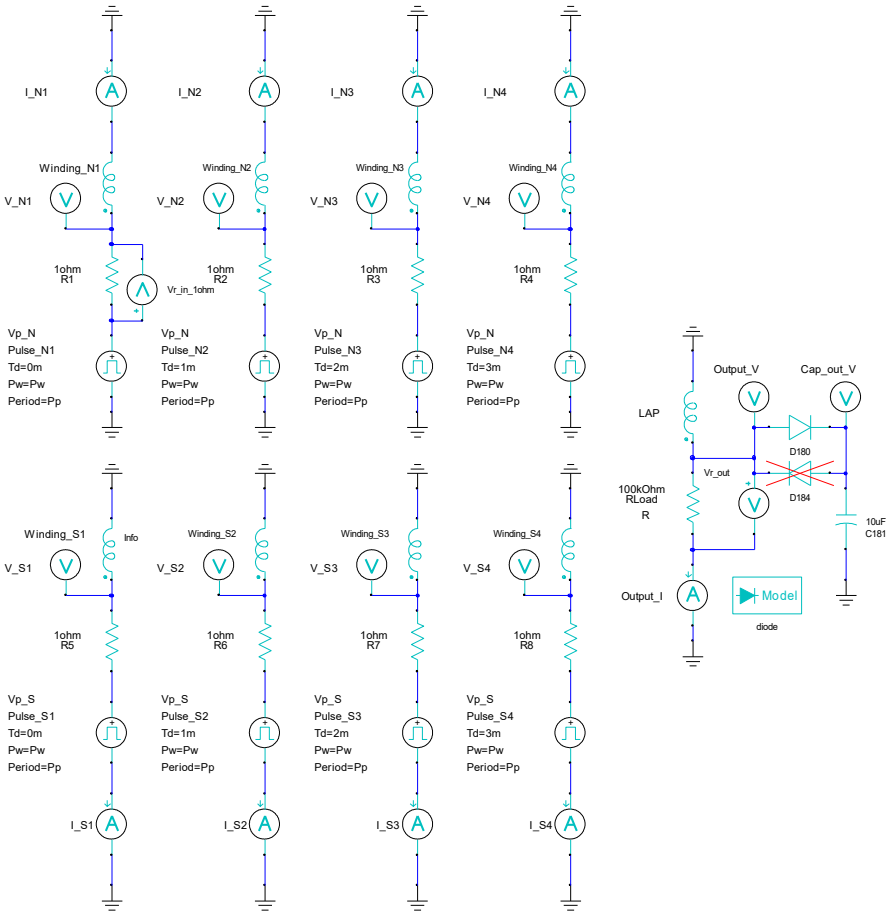
Therefore; although the device is quite small (3" x 5" x 0.4"), it can pack a **lethal** punch, so to speak! It's not a toy...

Use CAUTION since a light load on the LAP Coil Output can generate voltages exceeding 400Vpp.

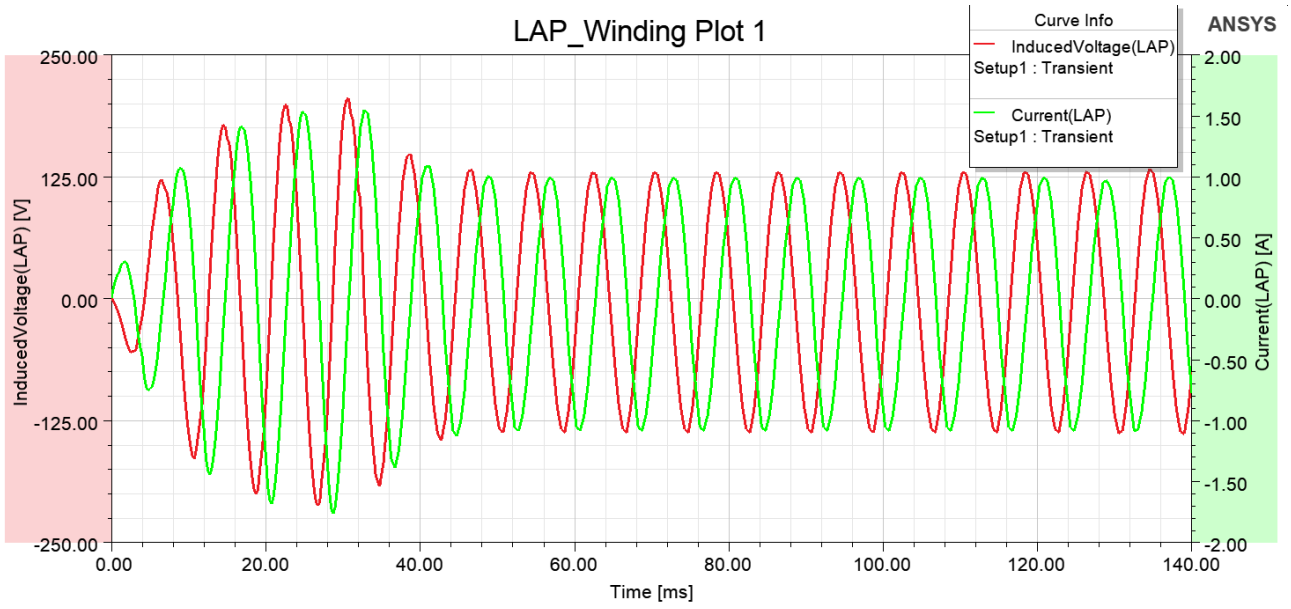
Note - Flyback recovery mechanism is not shown in this brief.



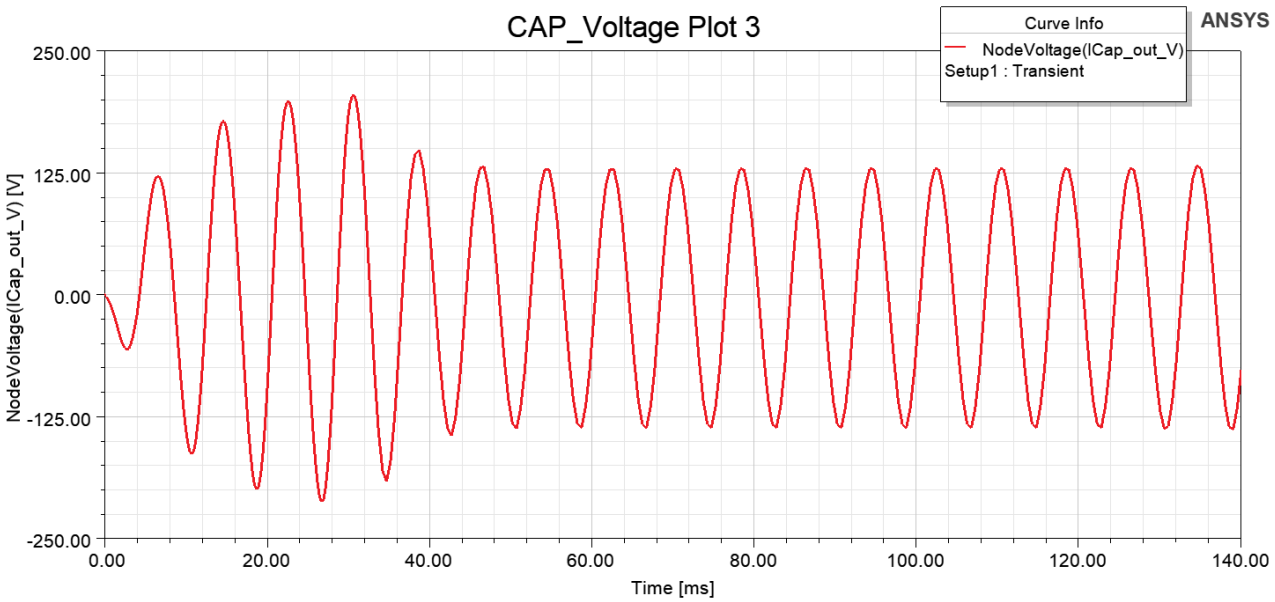
Output shown in the original block diagram (above) are from an older simulation.
Schematic and results below are from an updated (newer) simulator.



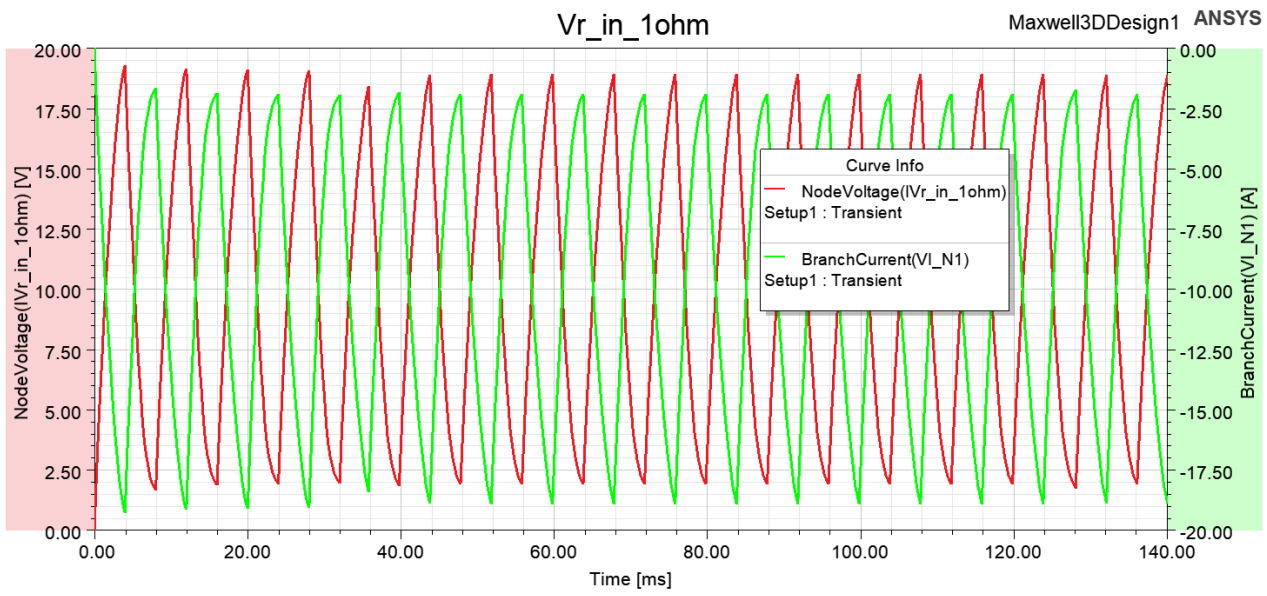
Vp = 20VDC Td = delay Pw = Pulse Width (8mS) Period = Period (4mS) [ideal components]



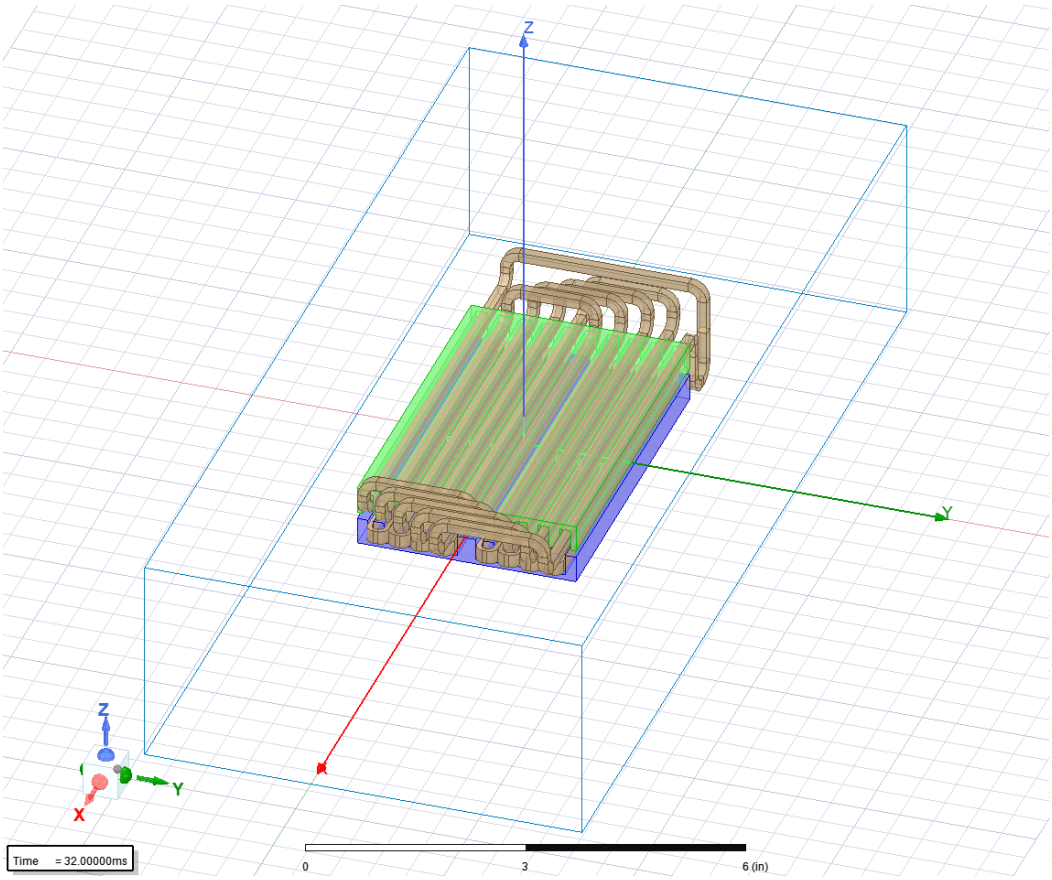
Output from the LAP Winding.



Voltage across Capacitor (at LAP Winding Output).



Inputs to N1-4 & S1-4 Pole Coils (only Ni is shown) from STM32 Micorprocessor (PWM) and MOSFET/Driver board.



3D Structure - Stator & Rotor Metal (approx 3" x 5" x0.4" total, 0.1" gap) [ChinaSteel-50CS470], Pole Coils (20 turns each) and LAP Coil (100 turns) [multi-strand Copper].