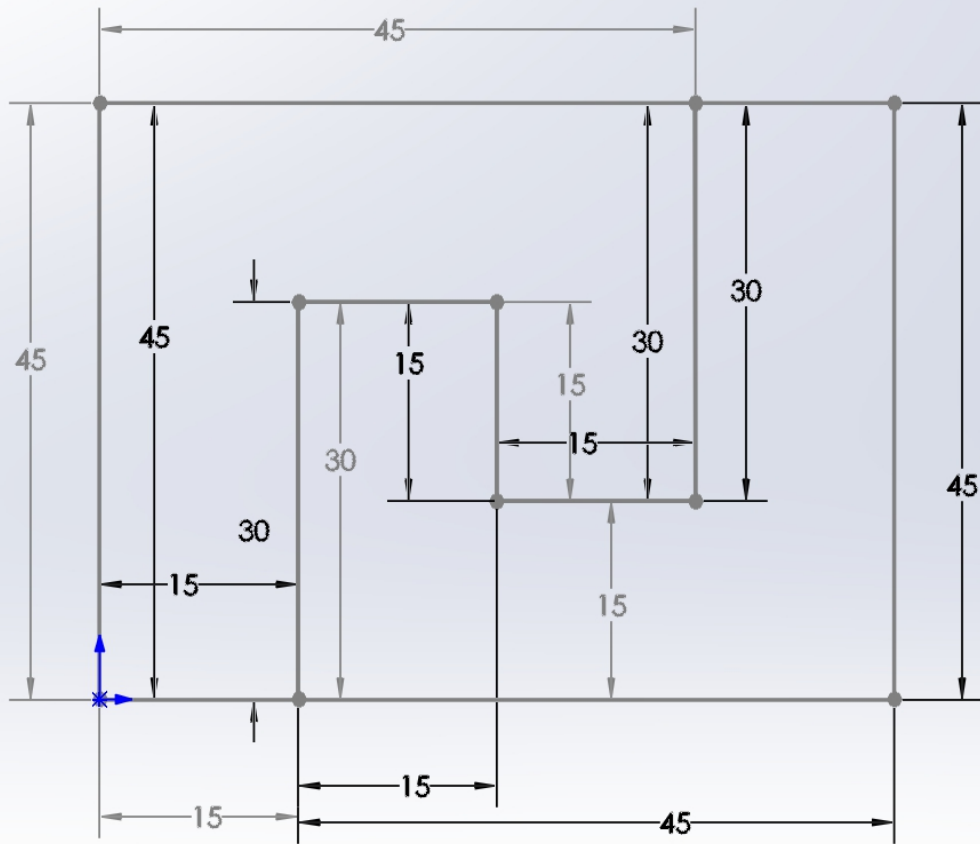


Lamination Orientation and Pole Spacing

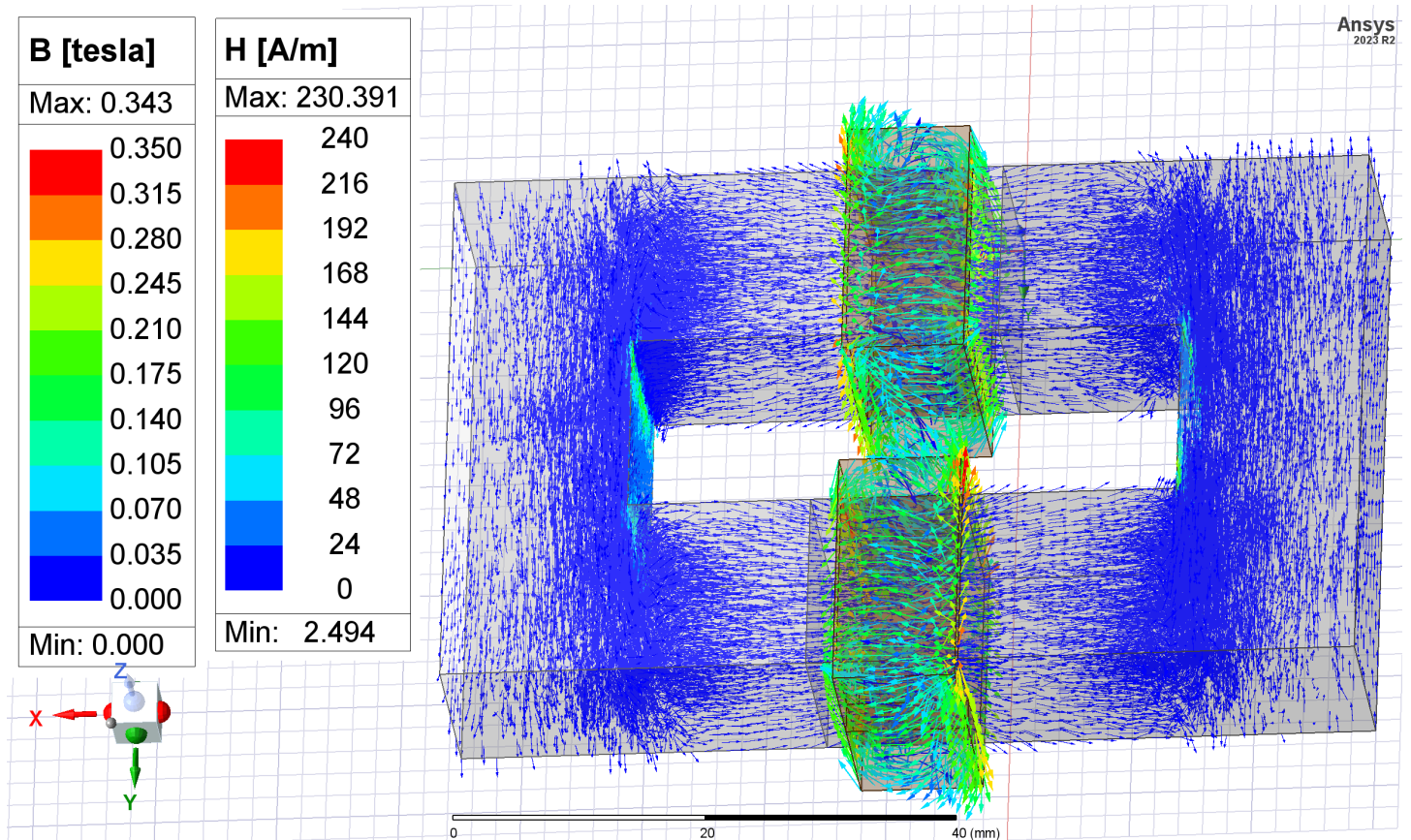
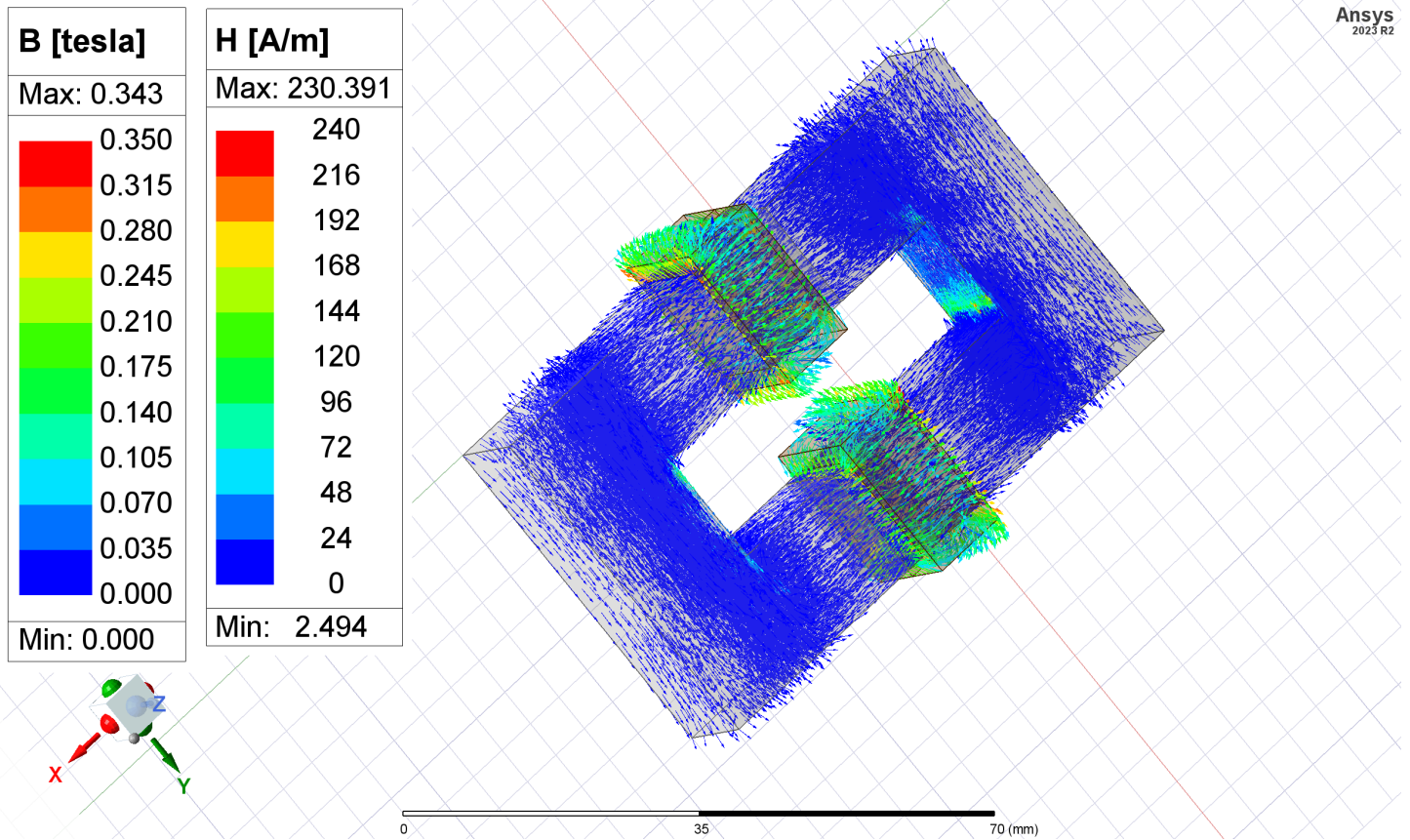
100mA 20turns *((simple design with little waste, but, not so good!))*

SEE Below - laminations appear to be set wrong - turned off - re-simulate - MUCH BETTER!

(this likely applies to the AEDT Student version also)



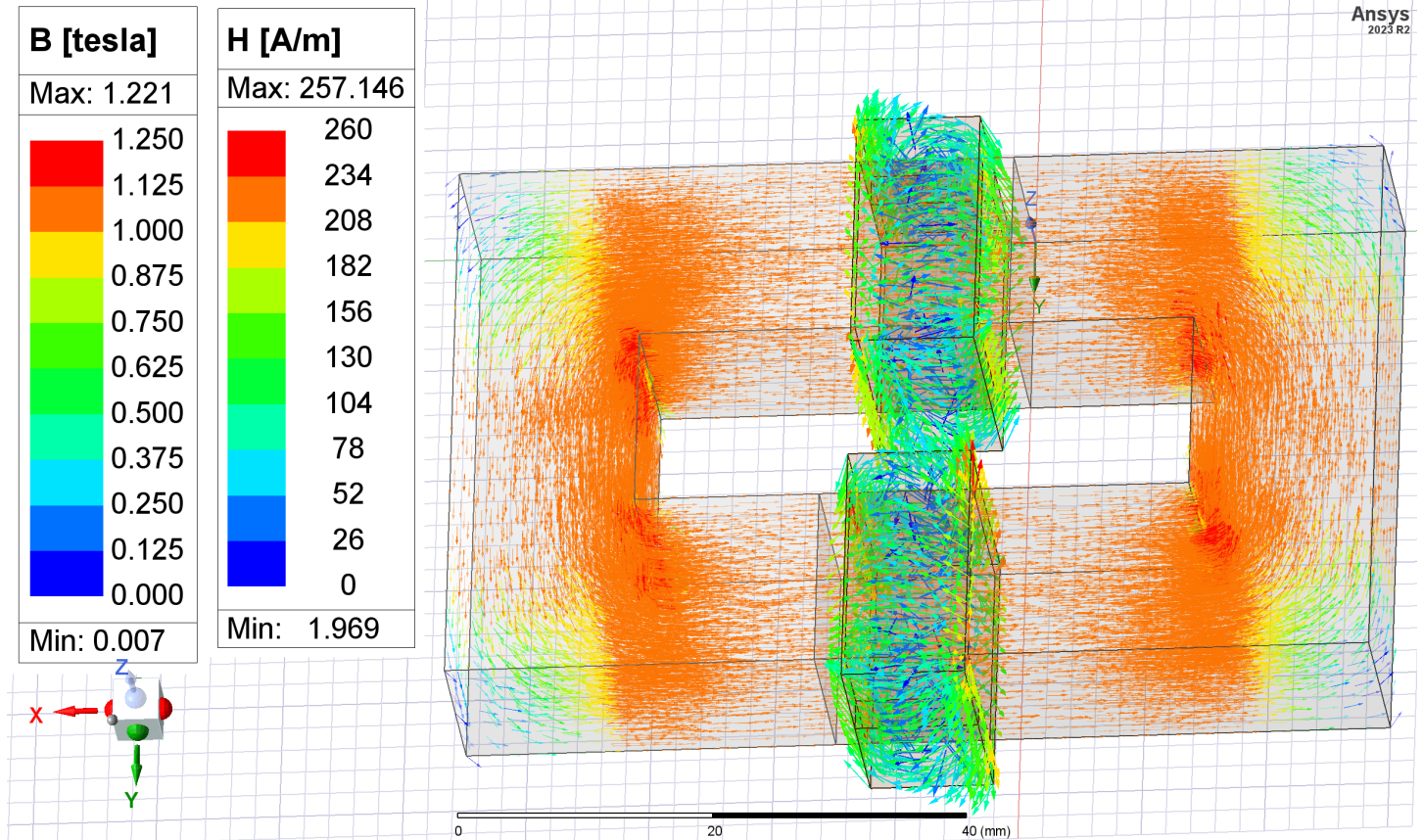
Results when the material Lamination direction is not set correctly:



=====

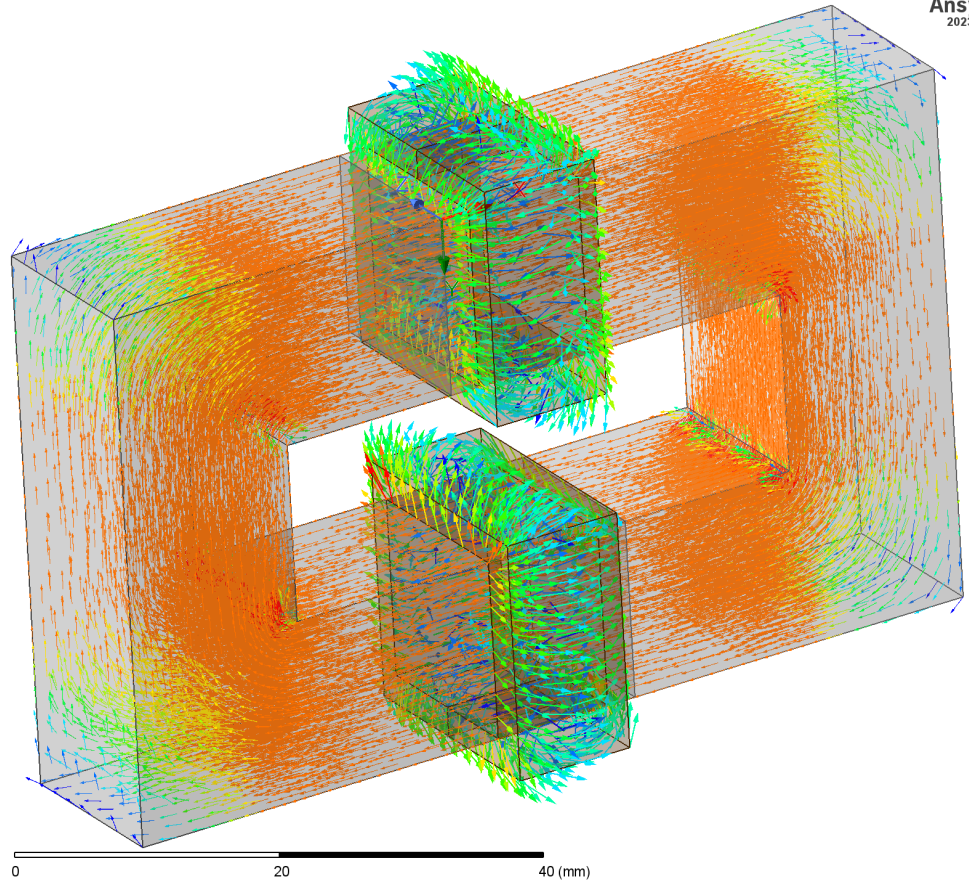
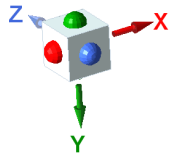
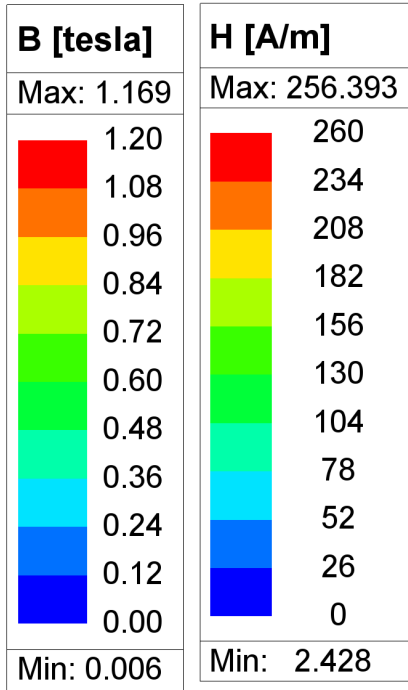
Lamination now turned off - (more study needed) [resolved - read the manual !]:

*** This might work OK *** **[[100mA 20 turns]]**

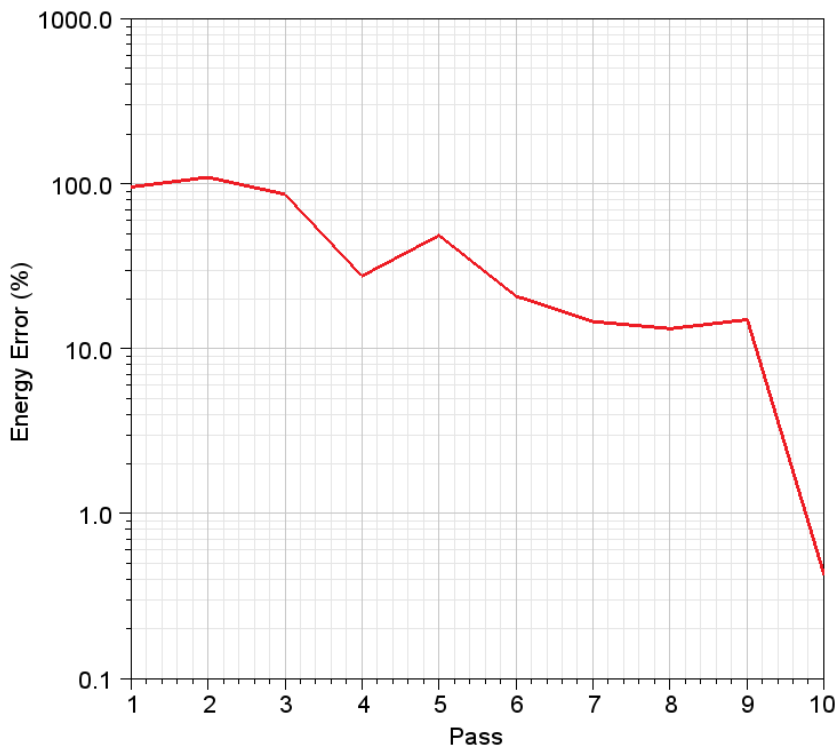


NOTE: Set the Lamination Stackin Direction to match the Global CS (in this case V3 or Z direction - came out OK)

Then tried Cosre Loss Model to Electrical Steel - seemed to work (same as above). {Kh, Kc, Ke & Kdc all = to 0}



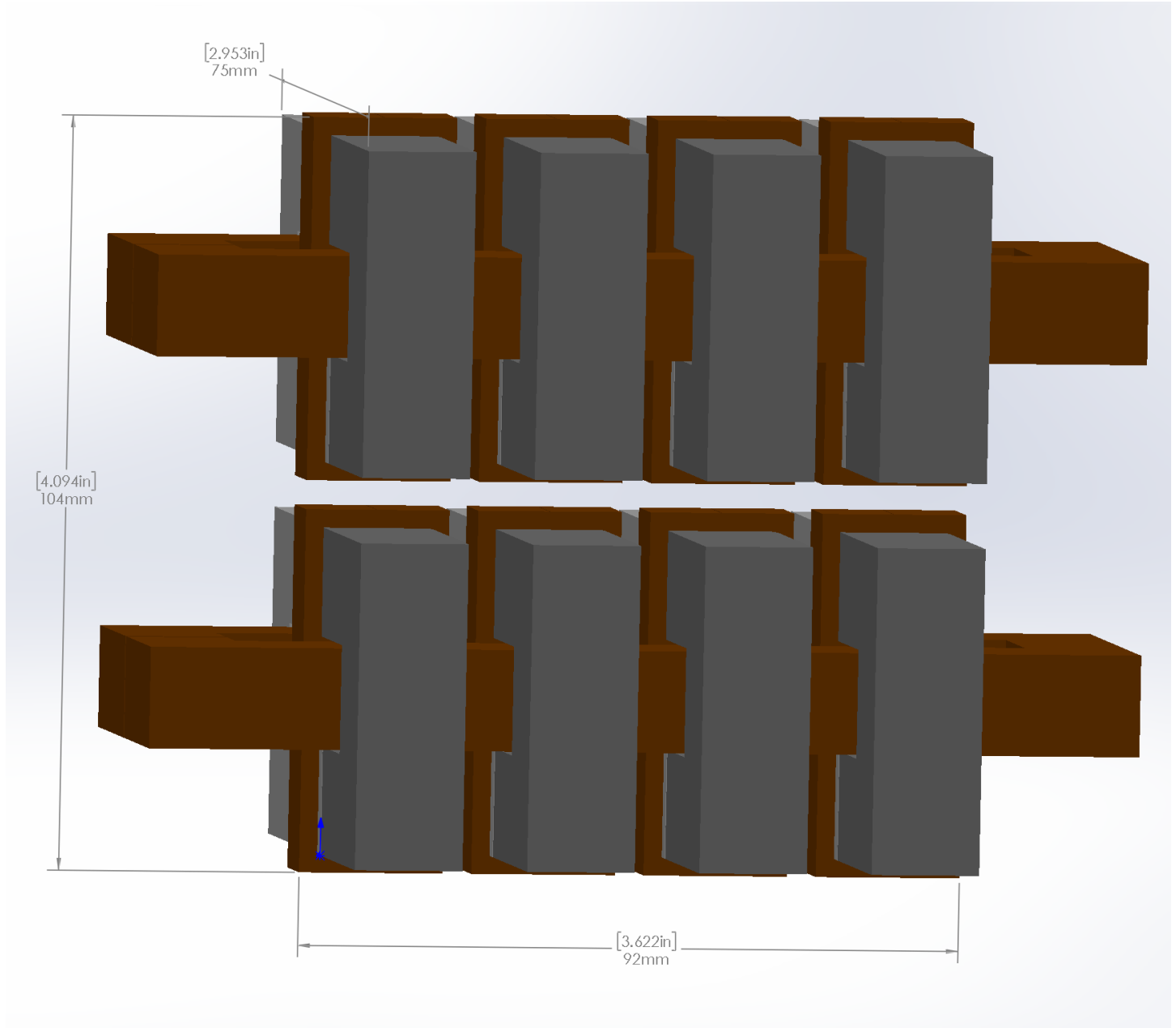
Convergence: (converges to less than 0.5%)

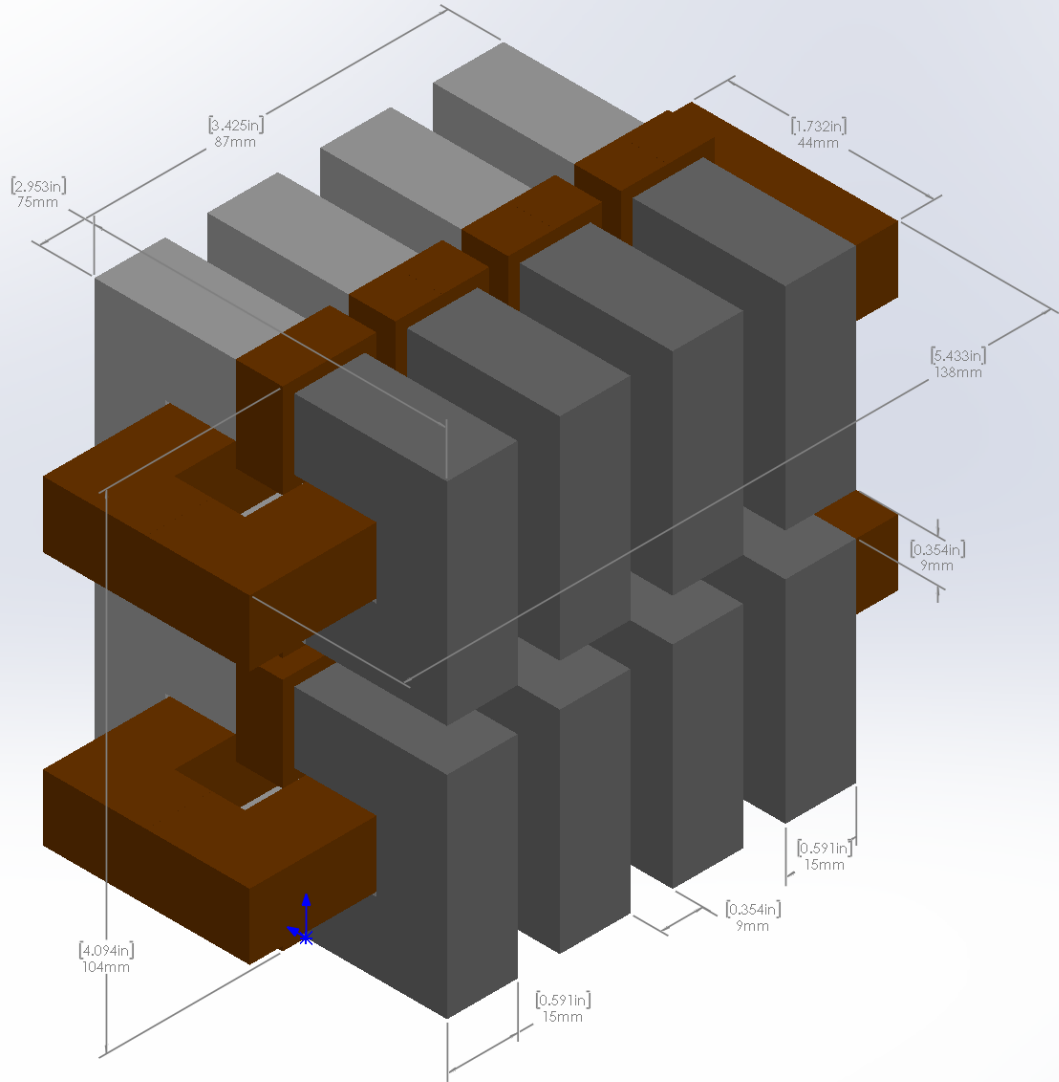


POLE SPACING

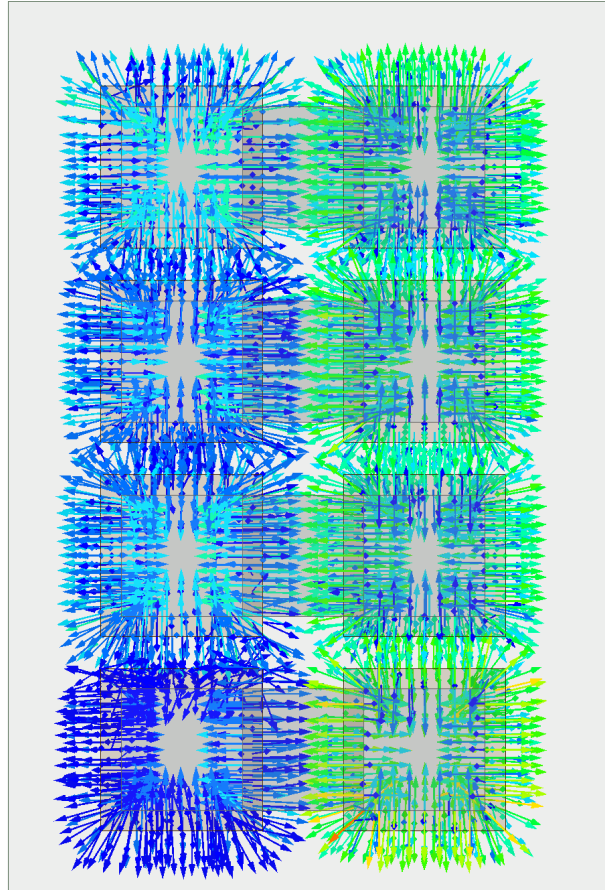
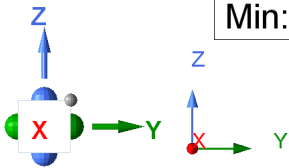
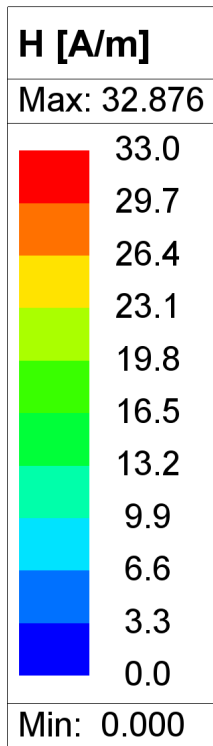
NOTE: This configuration may have failed (don't remember) since the Poles along the Loop were too close together - the adjacent N-N and S-S interfered with each other.

Pole to Pole spacing is about 9mm. This appears to be too close.



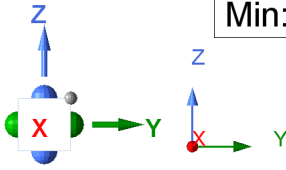
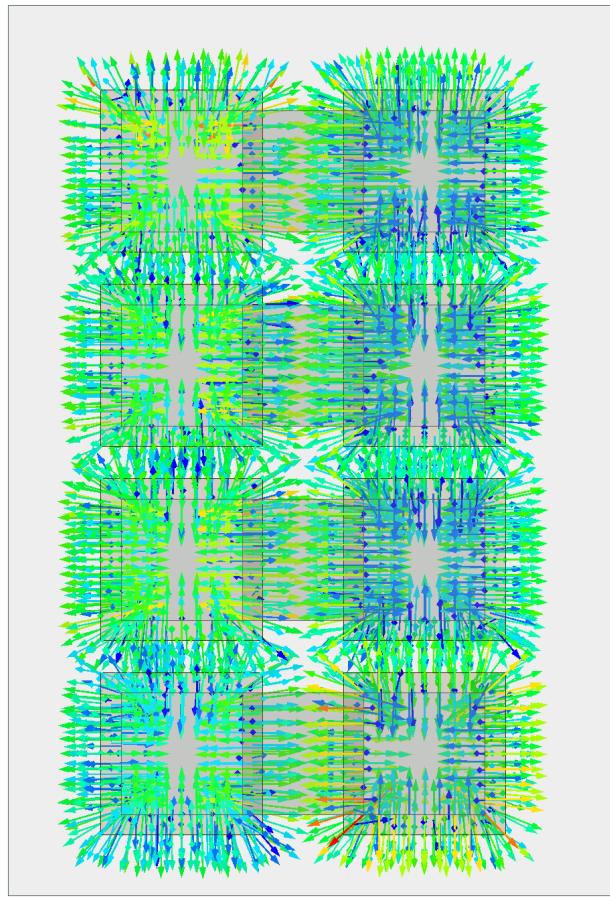
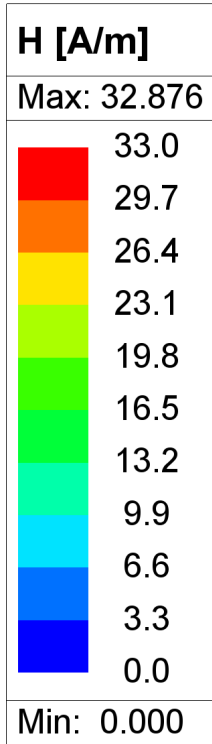


Pole spacing (see along the Z direction) is too close. The adjacent "B" fields interfere with each other:



Time = 9.5000ms

0 35 70 (mm)

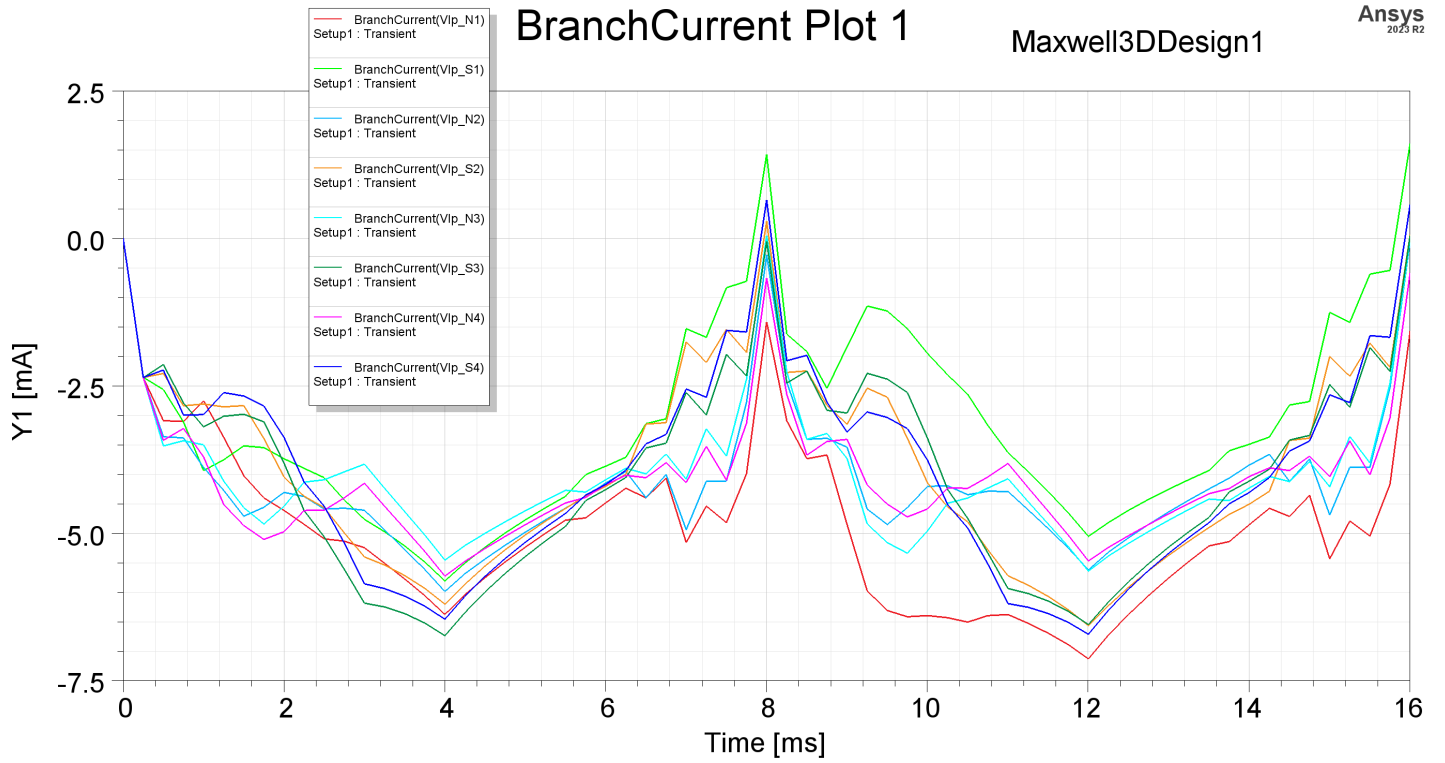


Time = 12.25000ms

0 35 70 (mm)

BranchCurrent Plot 1

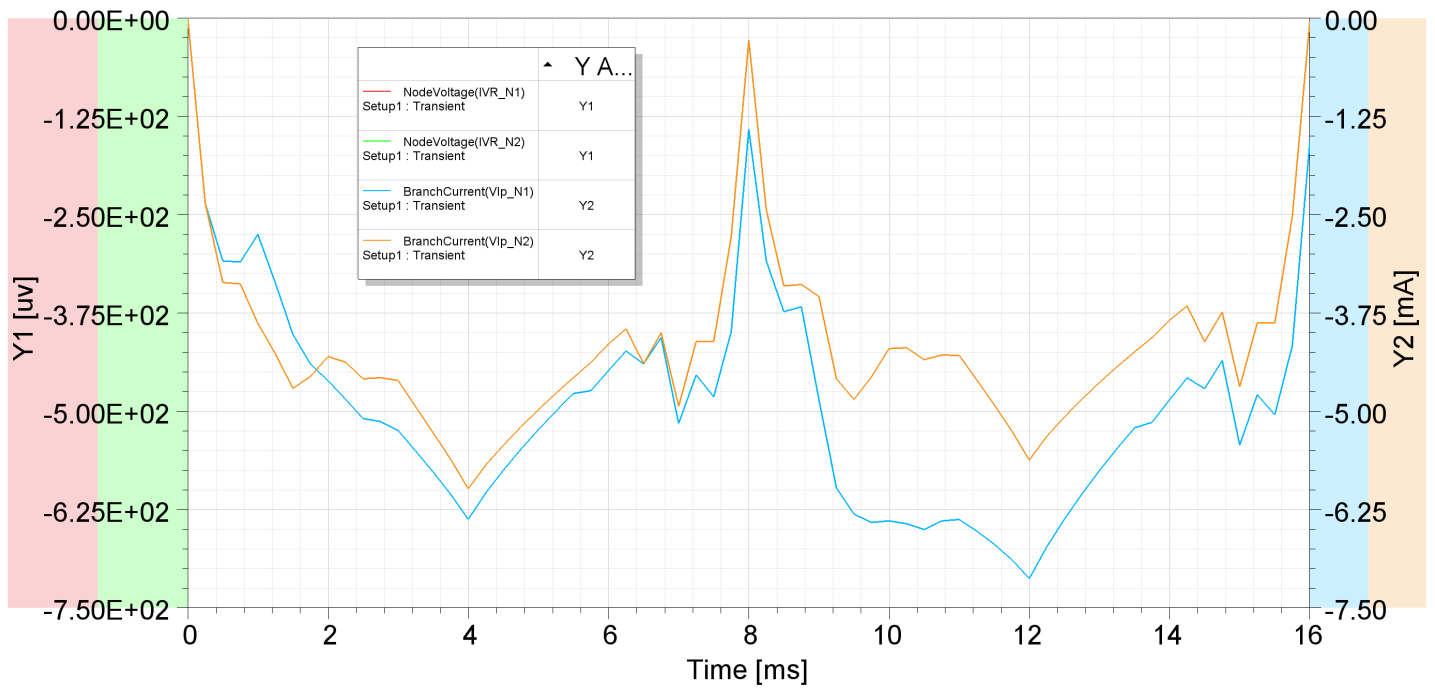
Maxwell3DDesign1



NodeVoltage Plot 1

Maxwell3DDesign1

Ansys
2023 R2



NOTES:

1. The material "Lamination Stack direction" is important. Ensure that the correct direction of lamination is selected [Y1, Y2, or Y3] when analyzing the device. This is set under "Properties, Material, etc." Otherwise the Analysis might not give proper results!

2. Pole spacing along the Loop is also a consideration as shown above.

SL